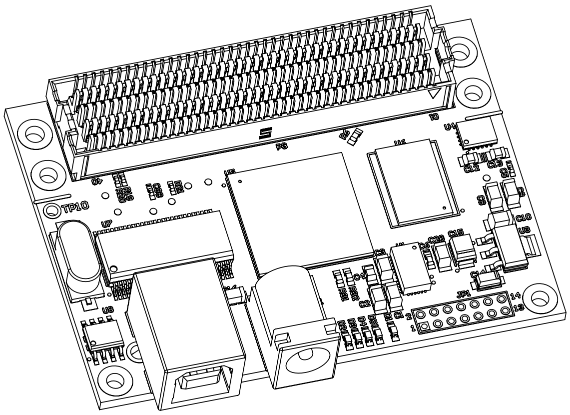


# Shuttle LX1 User's Manual

A compact (69mm x 50mm) Xilinx Spartan-6 FMC
Carrier with high-speed USB 2.0 interface and
1 Gb DDR2 SDRAM.

The Shuttle LX1 is a compact USB 2.0 FPGA integration module featuring the Xilinx Spartan-6 FPGA, 1 Gb (64 Mx16-bit) DDR2 SDRAM, high-efficiency switching power supplies, and a single FMC-LPC (FPGA mezzanine connector, low pin count) expansion connector. The high-speed USB 2.0 interface provides fast configuration downloads and PC-FPGA communication as well as easy access with our popular FrontPanel application and SDK.

Opal Kelly Incorporated
Portland, Oregon
http://www.opalkelly.com



Revision History:

| Date | Description |
|---|---|
| 20111017 | Initial release. |
| 20120207 | Added JTAG connection diagram and references in FMC pinout. |

# Contents

# Introducing the Shuttle LX1

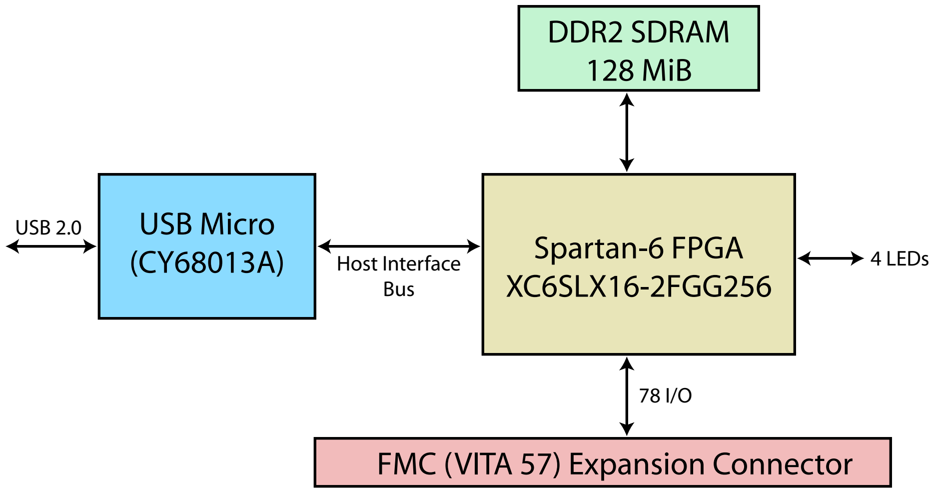
The Shuttle LX1 is a compact FPGA board featuring the Xilinx Spartan-6 FPGA and high-speed USB 2.0 connectivity. Designed as a full-featured integration system, the Shuttle LX1 provides access to up to 78 I/O pins on its 484-pin Spartan-6 device and has a 128-MiByte DDR2 SDRAM available to the FPGA. The Shuttle LX1 is designed for medium-sized FPGA designs with a wide variety of external interface requirements.

Note: The Shuttle LX1 is also known as the XEM6006 and the names may be used interchangeably.

## PCB Footprint

A mechanical drawing of the Shuttle LX1 is shown at the end of this manual. The PCB is 69mm x 50mm with four mounting holes (M2 metric screws) spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the Shuttle LX1. Two additional mounting holes are available for mechanical mating to the FMC module per the Vita-57 specification. The two connectors (USB and DC power) overhang the PCB by approximately 4mm in order to accommodate mounting within an enclosure.

## Functional Block Diagram




## FPGA

The off-the-shelf Shuttle LX1 has the LX16 FPGA density. Two additional densities are compatible with the Shuttle LX1 design and are available for quantity orders. The table below lists some of the differences between the two devices. Please consult the Xilinx documentation for a more thorough comparison.

| Feature | XEM6006-LX16 | XEM6006-LX25 |
|---|---|---|
| FPGA | XC6SLX16-2FGG256C | XC6SLX25-2FGG256C |
| Slice Count | 2,278 | 3,758 |
| Flip-Flops | 18,224 | 30,064 |
| Distributed RAM | 136 Kib | 229 Kib |
| Block RAM | 576 Kib | 936 Kib |
| DSP Slices | 32 | 38 |
| Clock Management Tiles | 2 | 2 |

## Power Supply

The Shuttle LX1 is designed to be operated from a 5-volt power source supplied through the DC power jack on the device or the expansion connectors on the bottom of the device. This provides power for the following power supplies:

- 3-A, 3.3-v switching regulator
- 1-A, 1.8-v switching regulator
- 1-A, 1.2-v low-dropout linear regulator
- 2-A, Adjustable voltage switching regulator for FMC $V_{ADJ}$
- 0.9-v low-dropout linear regulator for DDR2 termination voltage

### DC Power Connector

The DC power connector on the Shuttle LX1 is part number PJ-102AH from CUI, Inc. It is a standard "cannon-style" 2.1mm / 5.5mm jack. The outer ring is connected to DGND. The center pin is connected to +VDC.

## High-Speed USB 2.0 Interface

The Shuttle LX1 uses a Cypress CY7C68013A FX2LP USB microcontroller to make the XEM a USB 2.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

## On-board Peripherals

The Shuttle LX1 is designed to compactly support a large number of applications with a small number of on-board peripherals. These peripherals are listed below.

### 128-MByte Word-Wide DDR2 Synchronous DRAM

The XEM also includes a 128-MiByte DDR2 SDRAM with a full 16-bit word-wide interface to the FPGA. This SDRAM is attached exclusively to the FPGA and does not share any pins with the expansion connector. The maximum clock rate of the SDRAM is 333 MHz. With the -2 speed grade of the Spartan-6, the maximum clock rate is 312.5 MHz for a supported peak memory bandwidth of 10 Gb/s.

The DDR2 SDRAM is a Micron MT47H64M16HR-3:H (or compatible).

### LEDs

Four LEDs and are available for general use as debug outputs.

## FMC Expansion Connector

FMC (FPGA Mezzanine Connector) is the common name for the VITA 57 specification which describes a common connector design to interface large pin-counts to devices with configurable I/O such as an FPGA. The specification is available for purchase through the VITA website:

**http://www.vita.com/fmc.html**

The Shuttle LX1 specifically supports the LPC (low pin-count) version of the specification. For details on supported FMC features, please see the FMC Feature Support section.

FMC connectors are manufactured by Samtec. The FMC connector on the Shuttle LX1 is the Samtec ASP-134603-01. The mating connector which would appear on an FMC module is the Samtec ASP-134604-01. These are both surface-mount pin-field-array style connectors. The connectors ship with a solder plug on each connector which melts during reflow to the solder paste spread on the bare board for assembly. Connector contact is solid and insertion and removal forces are relatively small. High frequency performance is up to 9.5 GHz in single-ended operation and to 10.5 GHz in differential operation.

## FrontPanel Support

The Shuttle LX1 is fully supported by Opal Kelly's FrontPanel Application. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds tremendous value to the Shuttle LX1 as a device evaluation platform, general-purpose experimentation, or prototyping system.

### Programmer's Interface

In addition to complete support within FrontPanel, the Shuttle LX1 is also fully supported by the FrontPanel SDK, a powerful C++ class library available to Windows, Mac OS X, and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for C#, Java, and Python making the API available under those languages as well. The Opal Kelly community has also successfully used our API from within third-party environments such as Matlab and LabVIEW.

Complete documentation and several sample programs are installed with FrontPanel.

# *Applying the Shuttle LX1*

## Powering the Shuttle LX1

The Shuttle LX1 requires that this supply be clean, filtered, and within the range of 4.5v to 5.5v. This supply must be delivered through the power connector on-board.

### Power Budget

The table below can help you determine your power budget for each supply rail on the Shuttle LX1. All values are highly dependent on the application, speed, usage, and so on. Entries we have made are based on typical values presented in component datasheets or approximations based on Xilinx power estimator results. Shaded boxes represent unconnected rails to a particular component. Empty boxes represent data that the user must provide based on power estimates.

The user may also need to adjust parameters we have already estimated (such as FPGA $V_{CCO}$ values) where appropriate.

Note that $V_{ADJ}$ is provided to the FMC as a programmable voltage selected by an EEPROM present on the peripheral module. The maximum current available to this device is two amps. 3.3v is also provided to the FMC mezzanine module with some current consumed on the Shuttle LX1 by the USB interface, the FPGA's $V_{CCAUX}$ supply, and the DDR2 termination voltage regulator.

| Component(s) | 1.2v | 1.8v | 3.3v | $V_{ADJ}$ (2 Amp) |
|---|---|---|---|---|
| USB 2.0 | | | 280 mW | |
| DDR2 | | 600 mW | 250 mW | |
| FPGA $V_{CCINT}$ | | | | |
| FPGA $V_{CCAUX}$ | | | 250 mW | |
| FPGA $V_{CCO1}$ (DDR2), est. | | 250 mW | | |
| FPGA $V_{CCO2}$ (USB), est. | | | 100 mW | |
| FPGA $V_{CCO0,3}$ | | | | |
| FMC Mezzanine Module | | | | |
| **Total:** | | | | |
| **Available:** | 1,200 mW | 1,800 mW | 9,900 mW | |

## Example XEM6006-LX16 FPGA Power Consumption

XPower Estimator version 12.3 was used to compute the following power estimates for the $V_{CCINT}$ supply. These are simply estimates; your design requirements may vary considerably. The numbers below indicate approximately 70% to 80% utilization.

| Component | Parameters | $V_{CCINT}$ |
|---|---|---|
| Clock | 150 MHz GCLK - 7,200 fanout | 42 mW |
| Clock | 100 MHz GCLK - 7,200 fanout | 28 mW |
| Logic (DFF) | 150 MHz, 7,200 DFFs | 39 mW |
| Logic (DFF) | 100 MHz, 7,200 DFFs | 24 mW |
| Logic (LUT) | 150 MHz, 3,600 Combinatorial, 100 SR, 100 RAM | 32 mW |
| Logic (LUT) | 100 MHz, 3,600 Combinatorial, 100 SR, 100 RAM | 21 mW |
| BRAM | 18-bit, 12 @ 150 MHz, 12 @ 100 MHz | 15 mW |
| DSP | 150 MHz, 25 slices | 14 mW |
| MCB | 150 MHz | 85 mW |
| Misc. | DCM, PLL, etc. | 50 mW |
| | **Total:** | 350 mW |
| | **Available:** | 1,200 mW |

## Supply Heat Dissipation (IMPORTANT!!)

Due to the limited area available on the small form-factor of the Shuttle LX1 and the density of logic provided, heat dissipation may be a concern. This depends entirely on the end application and cannot be predicted in advance by Opal Kelly. Heat sinks may be required on any of the devices on the Shuttle LX1. Of primary focus should be the FPGA (U5) and SDRAM (U6). Although the switching supplies are high-efficiency, they are very compact and consume a small amount of PCB area for the current they can provide.

If you plan to put the Shuttle LX1 in an enclosure, be sure to consider heat dissipation in your design.

## Host Interface

There are 26 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHost module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. Please see the sample projects included with your FrontPanel installation for examples.

## LEDs

In addition to the power LED, there are four LEDs attached to the FPGA. Each is wired directly to the FPGA according to the pin mapping tables at the end of this document.

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA on Bank 2 with a bank I/O voltage of 3.3v. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be at logic '1'.

## DDR2 SDRAM

The Micron DDR2 SDRAM is connected exclusively to the 1.8-v I/O on Bank 1 of the FPGA. The following tableslist these connections.

| DDR2 Pin | FPGA Pin |
|---|---|
| CK | G12 |
| $\overline{CK}$ | H11 |
| CKE | D14 |
| $\overline{CS}$ | F12 |
| $\overline{RAS}$ | J13 |
| $\overline{CAS}$ | K14 |
| $\overline{WE}$ | E15 |
| LDQS | N14 |
| $\overline{LDQS}$ | N16 |
| UDQS | R14 |
| $\overline{UDQS}$ | T15 |
| LDM | K11 |
| UDM | K12 |
| ODT | H14 |
| A0 | H15 |
| A1 | H16 |
| A2 | F16 |
| A3 | H13 |
| A4 | C16 |
| A5 | J11 |
| A6 | J12 |
| A7 | F15 |
| A8 | F13 |

| DDR2 Pin | FPGA Pin |
|---|---|
| A9 | F14 |
| A10 | C15 |
| A11 | G11 |
| A12 | D16 |
| BA0 | G14 |
| BA1 | G16 |
| BA2 | E16 |
| D0 | L14 |
| D1 | L16 |
| D2 | M15 |
| D3 | M16 |
| D4 | J14 |
| D5 | J16 |
| D6 | K15 |
| D7 | K16 |
| D8 | P15 |
| D9 | P16 |
| D10 | R15 |
| D11 | R16 |
| D12 | T14 |
| D13 | T13 |
| D14 | R12 |
| D15 | T12 |

## Clock Configuration (Source Synchronous)

The DDR2 clocking is designed to be source-synchronous from the FPGA. This means that the FPGA sends the clock signal directly to the SDRAM along with control and data signals, allowing very good synchronization between clock and data.

## Memory Controller Blocks

Spartan-6 has integrated memory control blocks to communicate with the external DDR2 memory on the Shuttle LX1. This is instantiated using the Xilinx Core Generator (memory interface generator, or MIG) to create a suitable memory controller for your design. You should read and become familiar with the DDR2 SDRAM datasheet as well as MIG and the core datasheet. Although MIG can save a tremendous amount of development time, understanding all this information is critical to building a working DDR2 memory interface.

The XEM6006 provides 1.2v as $V_{CCINT}$. According to the memory controller block documentation, the Spartan-6, -2 speed grade can operate memory to 312.5 MHz with this internal voltage.

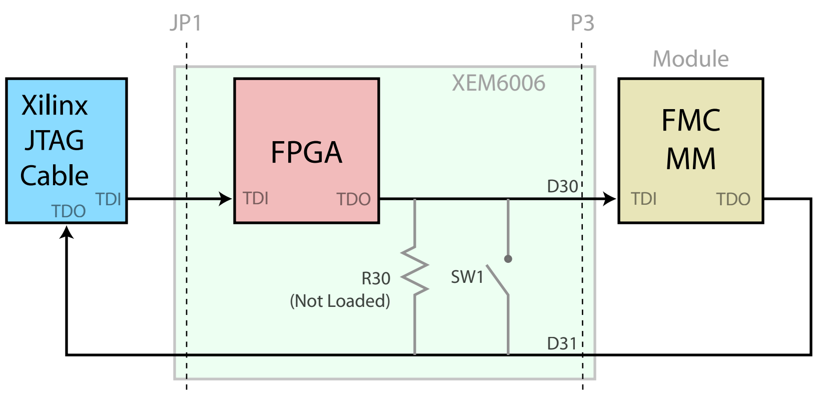
## MIG Settings

The following are the settings used to generate the MIG core for our RAMTester sample using Xilinx Core Generator. These settings were used with ISE 12.2 and MIG 2.3. Note that settings may be slightly different for different versions of ISE or MIG.

| | | |
|---|---|---|
| Frequency | 312.5 MHz | |
| Memory Type | Component | |
| Memory Part | MT47H64M16XX-3 (1Gb, x16) | |
| Data Width | 16 | |
| Enable DQS Enable | CHECKED | |
| High-temp self-refresh | DISABLED | |
| Output drive strength | Reducedstrength | |
| RTT(nominal) | 50 ohms | [default] |
| DCI for DQ/DQS | CHECKED | |
| DCI for address/control | CHECKED | |
| ZIO pin | L12 | |
| RZQ pin | E13 | |
| Calibrated Input Selection | Yes | |
| Class for address/control | Class II | |
| Debug signals | Your option | |
| System clock | Single-ended | |

## JTAG (JP1)

The JTAG connections on the FPGA and FMC connector are wired to JP1 as shown in the diagram below. This connector is not populated by default, but may be populated with Molex 87831-1420 or equivalent (2-mm, 14-position shrouded connector). The Molex part is compatible with the Xilinx JTAG cable.




The FMC module is designed to complete the JTAG chain. However, if a module is not present or it does not properly complete the chain, the chain may be bypassed using SW1. Additionally, a 0-Ω resistor may be installed at R30 to bypass the chain.

## FMC Expansion Connector (P3)

The FMC expansion connector (P3) is a Samtec ASP-134603-01, FMC LPC carrier connector. It is the specified connector the LPC versions of the FMC / VITA 57 specification and is compatible with the corresponding LPC mezzanine connector, Samtec ASP-134604-01.

The ASP-134603-01 is a 0.5-mm pitch pin grid array connector. In raw form, it is a terminal assembly whereby each pin has a solder plug at the board-side base. The PCB footprint is specified by the appropriate Samtec documentation and is similar to a BGA device footprint with surface-mount pads. The solder plug is designed to melt just like BGA solder balls and attach the terminals to the PCB. Despite the high pin-count, this connector has low insertion and removal forces, provides good connectivity, and very good high-frequency performance.

## PCB Design Recommendations

Opal Kelly suggests following manufacturer's recommendations for all footprint and assembly guidelines when designing your own FMC mezzanine modules. However, the following remarks may prove helpful.

Samtec suggests using a 6-mil solder stencil when assembling boards with the FMC connectors. Assembly of other components with fine geometry such as QFN packages may benefit from the more standard 5-mil solder stencil. In this case, Opal Kelly has had good success in expanding the FMC stencil apertures from their specified round aperture to a 0.037-inch square aperture with 0.003-inch rounded corners. The increase in paste application from aperture makes up for the reduced paste volume from the thinner stencil.

## Setting I/O Voltages

The FMC specification is designed to allow the FMC mezzanine module to determine the interface voltage by communicating the desired $V_{ADJ}$ voltage at start-up. This is done by programming the desired settings into a small $I^2C$ EEPROM following the IPMI specification with details in the FMC specification. Opal Kelly provides an online tool for generating compliant EEPROM binaries at the following URL:

**http://www.opalkelly.com/tools/FMCEepromGenerator.php**

If an EEPROM on-board is not available or desired, the FMC system controller on the Shuttle LX1 provides a manual mode to override this type of $V_{ADJ}$ specification. To configure these modes, Opal Kelly provides an executable tool called `fmcconfig` and FPGA configuration bitfile. Please see the `fmcconfig` sample in the FrontPanel SDK for usage information.

## Considerations for Differential Signals

The Shuttle LX1 PCB layout and routing has been designed with several applications in mind, including applications requiring the use of differential (LVDS) pairs. Please refer to the Xilinx Spartan-6 datasheet for details on using differential I/O standards with the Spartan-6 FPGA.

Note: LVDS output on the Spartan-6 is restricted to banks 0 and 2. LVDS input is available on all banks. For more information, please refer to the *Spartan-6 FPGA SelectIO Resources User Guide* from Xilinx.

### FPGA I/O Bank Voltages

In order to use differential I/O standards with the Spartan-6, you must set the VCCO voltages for the appropriate banks to 2.5v according to the Xilinx Spartan-6 datasheet. Please see the section above entitled "Setting I/O Voltages" for details.

### Characteristic Impedance

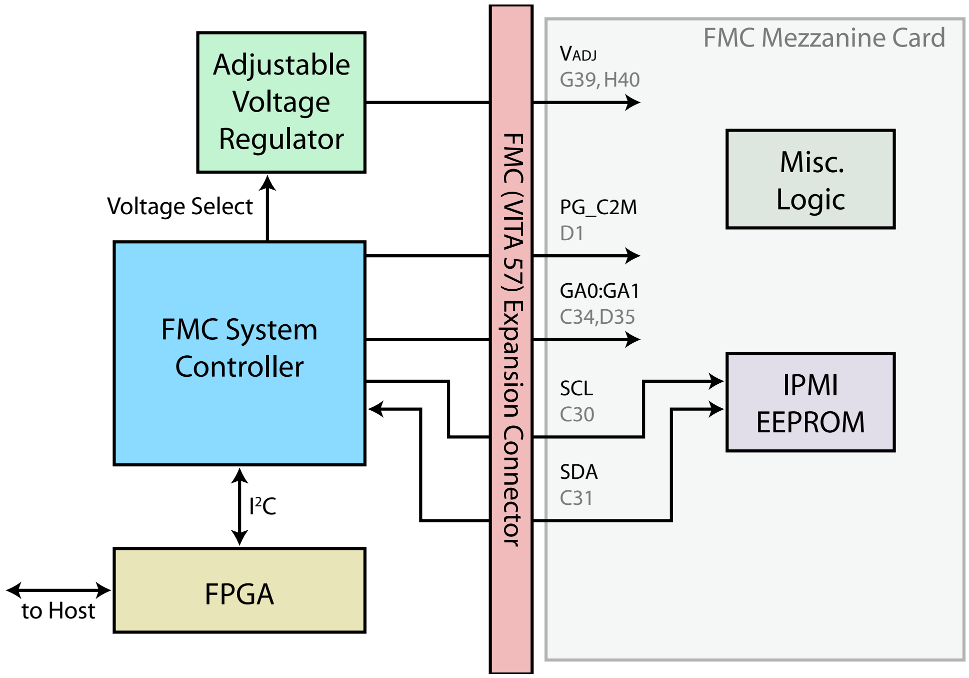
The characteristic impedance of all routes from the FPGA to the expansion connector is approximately 50-Ω.

### Differential Pair Lengths

In many cases, it is desirable that the route lengths of a differential pair be matched within some specification. Care has been taken to route differential pairs on the FPGA to adjacent pins on the expansion connectors whenever possible. We have also included the lengths of the board routes for these connections to help you equalize lengths in your final application. Due to space constraints, some pairs are better matched than others.

## FMC System Controller

The FMC specification provides for a system controller to communicate over the I²C signals to a small EEPROM on the mezzanine device for identification and settings such as VADJ voltage. On the Shuttle LX1, this system controller role is served by a small microcontroller as shown in the diagram below.




The system controller manages four items:

- FMC Geographical Address (GA1:GA0)
- Switching regulator to set the adjustable voltage level (VADJ)
- FMC Power Good signal (PG_C2M) to mezzanine device
- Although not part of the FMC specification, the Shuttle LX1 also provides access to other I²C devices that may be on the mezzanine device.

### FMC Geographical Address

The FMC Geographical Address is two pins (GA1:GA0) that are typically used by a mezzanine device to determine which FMC connector on a carrier it is attached to. The Shuttle LX1 has only one FMC connector and therefore the default geographical address is 00. This default may be changed using the FlashLoader sample.

Some mezzanine cards may attach other devices to the I²C bus and address them through the system controller, using the geographical address as a chip-select. This is not strictly in adherence with the FMC specification, but the Shuttle LX1 allows it by providing I²C commands to set the geographical address dynamically.

## Adjustable Voltage

FMC specifies that $V_{ADJ}$ be adjustable using a "personality" EEPROM installed on the mezzanine board. This EEPROM should contain an IPMI-formatted personality which informs the system controller what voltage to use.

To make things simple and obviate the need for a full IPMI-formatted EEPROM on the mezzanine board, the Shuttle LX1 system controller allows the user to configure the $V_{ADJ}$ voltage applied using the FlashLoader sample.

## Startup Modes

The system controller has three modes of startup operation. The user can set the startup mode using the FlashLoader sample.

### Automatic

In this mode, the system controller boots and looks for an IPMI-formatted EEPROM attached to the FMC bus. If an FMC device is not attached or an IPMI-formatted EEPROM is not found, the system controller disables the adjustable voltage regulator and does not power $V_{ADJ}$.

The boot sequence in this mode is as follows:

- Set GA1:GA0 according to internal non-volatile settings.
- If a mezzanine board is not attached, disable $V_{ADJ}$ and STOP.
- If an IPMI-formatted EEPROM is not attached, disable $V_{ADJ}$ and STOP.
- Load $V_{ADJ}$ settings from the mezzanine board's EEPROM and set $V_{ADJ}$.
- Enter command processing mode to allow $I^2C$ communication pass-through as well as geographical address manipulation.

### Manual

When the Manual startup mode is selected, the system controller will ignore the existence of an EEPROM on the FMC bus and use the settings stored in an internal non-volatile memory to set $V_{ADJ}$ and the FMC Geographical Address.

The boot sequence in this mode is as follows:

- Set GA1:GA0 according to internal non-volatile settings.
- If a mezzanine board is not attached, disable $V_{ADJ}$ and STOP.
- Set $V_{ADJ}$ according to internal non-volatile settings.
- Enter command processing mode to allow $I^2C$ communication pass-through as well as geographical address manipulation.

### Fallback [Default]

The Fallback startup mode is a combination of Automatic and Manual modes and allows the system controller to look for an IPMI-formatted EEPROM for FMC settings. If found, those settings are applied. If not found, the settings stored in an internal non-volatile memory are used.

The boot sequence in this mode is as follows:

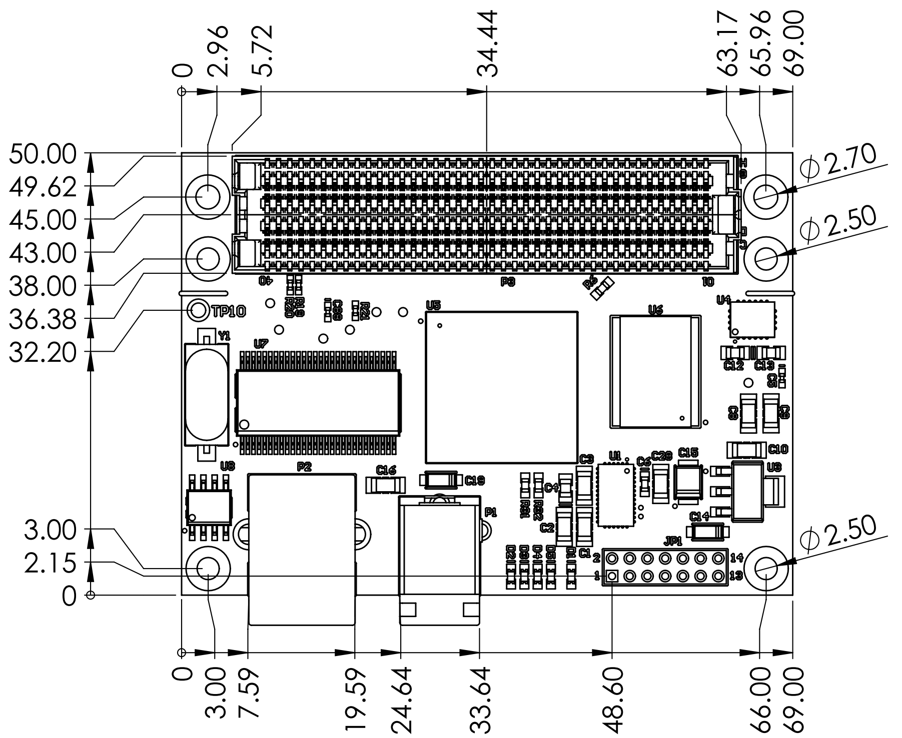
- Set GA1:GA0 according to internal non-volatile settings.
- If a mezzanine board is not attached, disable $V_{ADJ}$ and STOP.
- If an IPMI-formatted EEPROM is not attached, proceed with Manual startup procedure.
- Load $V_{ADJ}$ settings from the mezzanine board's EEPROM and set $V_{ADJ}$.
- Enter command processing mode to allow $I^2C$ communication pass-through as well as geographical address manipulation.

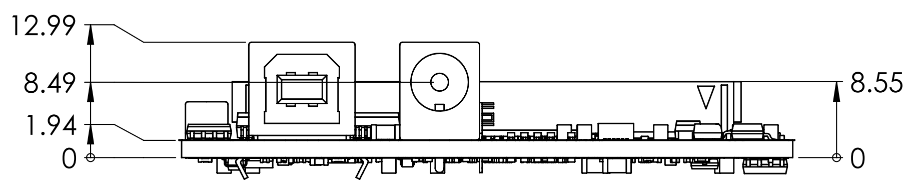
## FMC Compatibility Checklist

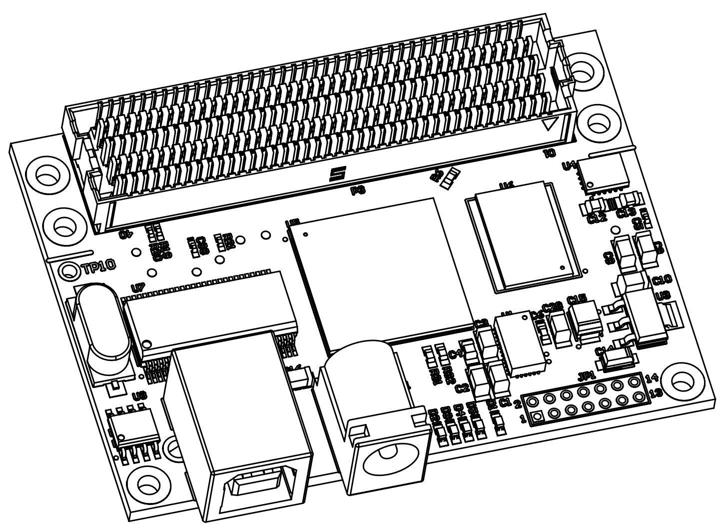
The specifications below are intended to help you determine compatibility between a specific FMC device and the Shuttle LX1 FMC carrier.

| Feature / Specification | Shuttle LX1 Support |
|---|---|
| FMC LPC pins available | LA[33:0]_P and LA[33:0]_N<br>LA[16:0] are on FPGA bank 0<br>LA[33:17] are on FPGA bank 3 |
| FMC HPC pins available | HPC not supported |
| Bank LA signaling standard support | See Xilinx Spartan-6 SelectIO User Guide<br>LVDS *input-only* for LA[16:0] on Bank 0<br>LVDS input and output for LA[33:17] on Bank 3 |
| 3P3V current available | Approximately 2.8A available to module |
| 12PV0 current available | User-supplied via TP10, if required |
| VADJ ranges allowed | 0.8, 1.2, 1.25, 1.5, 1.8, 2.5, 3.3 |
| VADJ current available | 2A |
| JTAG clock speed | 0 MHz to 33 MHz |
| Data line trace lengths for skew matching | LA[33:0], CLK[1:0] matched to within 1mm |
| CLK bank connections | CLK[1:0] are connected to GCLKs on Bank 3 |
| Source-synchronous clocking for _CC pins | LA[0, 1, 17, 18] are connected to GCLKs |

# Shuttle LX1 Mechanical Drawing



All dimensions in mm

# Shuttle LX1 Quick Reference

| P3 Pin | FMC Signal | FPGA Pin | FPGA Pad | Length (mm) |
|---|---|---|---|---|
| H1 | VREF_A_M2C | | Bank 0 & 3 VREF | |
| H2 | PRSNT_M2C_L | | | |
| H3 | GND | | | |
| H4 | CLK0_M2C_P | F2 | L41P_GCLK27_3 | 47.505 |
| H5 | CLK0_M2C_N | F1 | L41N_GCLK26_3 | 47.525 |
| H6 | GND | | | |
| H7 | LA02_P | D11 | L66P_0 | 32.795 |
| H8 | LA02_N | D12 | L66N_0 | 33.300 |
| H9 | GND | | | |
| H10 | LA04_P | F10 | L64P_0 | 26.544 |
| H11 | LA04_N | E11 | L64N_0 | 24.685 |
| H12 | GND | | | |
| H13 | LA07_P | C11 | L39P_0 | 21.140 |
| H14 | LA07_N | A11 | L39N_0 | 18.476 |
| H15 | GND | | | |
| H16 | LA11_P | D6 | L7P_0 | 22.390 |
| H17 | LA11_N | C6 | L7N_0 | 21.254 |
| H18 | GND | | | |
| H19 | LA15_P | D5 | L3P_0 | 24.344 |
| H20 | LA15_N | C5 | L3N_0 | 22.113 |
| H21 | GND | | | |
| H22 | LA19_P | E2 | L46P_3 | 25.675 |
| H23 | LA19_N | E1 | L46N_3 | 25.267 |
| H24 | GND | | | |
| H25 | LA21_P | H2 | L39P_3 | 28.572 |
| H26 | LA21_N | H1 | L39N_3 | 27.982 |
| H27 | GND | | | |
| H28 | LA24_P | K2 | L37P_3 | 31.318 |
| H29 | LA24_N | K1 | L37N_3 | 30.729 |
| H30 | GND | | | |
| H31 | LA28_P | C1 | L50P_3 | 22.691 |
| H32 | LA28_N | B1 | L50N_3 | 21.361 |
| H33 | GND | | | |
| H34 | LA30_P | D3 | L49P_3 | 27.510 |
| H35 | LA30_N | D1 | L49N_3 | 25.950 |
| H36 | GND | | | |
| H37 | LA32_P | E4 | L54P_3 | 31.766 |
| H38 | LA32_N | E3 | L54N_3 | 31.737 |
| H39 | GND | | | |
| H40 | VADJ | See FMC system controller section | | |

| JP2 Pin | FMC Signal | FPGA Pin | FPGA Pad | Length (mm) |
|---|---|---|---|---|
| G1 | GND | | | |
| G2 | CLK1_M2C_P | H4 | L44P_GCLK21_3 | 48.952 |
| G3 | CLK1_M2C_N | H3 | L44N_GCLK20_3 | 48.823 |
| G4 | GND | | | |
| G5 | GND | | | |
| G6 | LA00_P_CC | E10 | L37P_GCLK13_0 | 27.165 |
| G7 | LA00_N_CC | C10 | L37N_GCLK12_0 | 25.028 |
| G8 | GND | | | |
| G9 | LA03_P | B14 | L65P_0 | 18.890 |
| G10 | LA03_N | A14 | L65N_0 | 17.557 |
| G11 | GND | | | |
| G12 | LA08_P | B10 | L35P_GCLK17_0 | 18.451 |
| G13 | LA08_N | A10 | L35N_GCLK16_0 | 17.299 |
| G14 | GND | | | |
| G15 | LA12_P | C7 | L6P_0 | 19.171 |
| G16 | LA12_N | A7 | L6N_0 | 16.747 |
| G17 | GND | | | |
| G18 | LA16_P | B5 | L2P_0 | 17.389 |
| G19 | LA16_N | A5 | L2N_0 | 16.237 |
| G20 | GND | | | |
| G21 | LA20_P | K5 | L47P_3 | 29.334 |
| G22 | LA20_N | K6 | L47N_3 | 27.619 |
| G23 | GND | | | |
| G24 | LA22_P | G3 | L40P_3 | 25.537 |
| G25 | LA22_N | G1 | L40N_3 | 23.948 |
| G26 | GND | | | |
| G27 | LA25_P | J3 | L38P_3 | 28.203 |
| G28 | LA25_N | J1 | L38N_3 | 26.604 |
| G29 | GND | | | |
| G30 | LA29_P | G6 | L51P_3 | 28.863 |
| G31 | LA29_N | G5 | L51N_3 | 29.542 |
| G32 | GND | | | |
| G33 | LA31_P | L4 | L45P_3 | 33.472 |
| G34 | LA31_N | L5 | L45N_3 | 35.421 |
| G35 | GND | | | |
| G36 | LA33_P | F6 | L55P_3 | 31.015 |
| G37 | LA33_N | F5 | L55N_3 | 30.425 |
| G38 | GND | | | |
| G39 | VADJ | See FMC system controller section | | |
| G40 | GND | | | |

| LED | FPGA Pin |
|---|---|
| D2 | M12 |
| D3 | L10 |
| D4 | M9 |
| D5 | T3 |

# Shuttle LX1 Quick Reference

| P3 Pin | FMC Signal | FPGA Pin | FPGA Pad | Length (mm) |
|---|---|---|---|---|
| D1 | PG_C2M | | | |
| D2 | GND | | | |
| D3 | GND | | | |
| D4 | GBTCLK0_M2C_P | N3 | L34P_3 | 47.563 |
| D5 | GBTCLK0_M2C_N | N1 | L34N_3 | 47.547 |
| D6 | GND | | | |
| D7 | GND | | | |
| D8 | LA01_P_CC | E7 | L36P_GCLK15_0 | 26.651 |
| D9 | LA01_N_CC | E8 | L36N_GCLK14_0 | 25.216 |
| D10 | GND | | | |
| D11 | LA05_P | C13 | L63P_0 | 15.087 |
| D12 | LA05_N | A13 | L63N_0 | 13.062 |
| D13 | GND | | | |
| D14 | LA09_P | C9 | L34P_GCLK19_0 | 16.120 |
| D15 | LA09_N | A9 | L34N_GCLK18_0 | 13.698 |
| D16 | GND | | | |
| D17 | LA13_P | F7 | L5P_0 | 18.679 |
| D18 | LA13_N | E6 | L5N_0 | 17.696 |
| D19 | GND | | | |
| D20 | LA17_P_CC | J6 | L43P_GCLK23_3 | 22.184 |
| D21 | LA17_N_CC | H5 | L43N_GCLK22_3 | 20.911 |
| D22 | GND | | | |
| D23 | LA23_P | F4 | L53P_3 | 19.362 |
| D24 | LA23_N | F3 | L53N_3 | 18.772 |
| D25 | GND | | | |
| D26 | LA26_P | C3 | L48P_3 | 15.006 |
| D27 | LA26_N | C2 | L48N_3 | 15.037 |
| D28 | GND | | | |
| D29 | TCK | See JTAG section | | |
| D30 | TDI | See JTAG section | | |
| D31 | TDO | See JTAG section | | |
| D32 | 3P3VAUX | Connected to +3.3VDD | | |
| D33 | TMS | See JTAG section | | |
| D34 | TRST_L | See JTAG section | | |
| D35 | GA1 | See FMC system controller section | | |
| D36 | 3P3V | Connected to +3.3VDD | | |
| D37 | GND | | | |
| D38 | 3P3V | Connected to +3.3VDD | | |
| D39 | GND | | | |
| D40 | 3P3V | Connected to +3.3VDD | | |

| JP3 Pin | FMC Signal | FPGA Pin | FPGA Pad | Length (mm) |
|---|---|---|---|---|
| C1 | GND | | | |
| C2 | DP0_C2M_P | L3 | L36P_3 | 44.619 |
| C3 | DP0_C2M_N | L1 | L36N_3 | 42.635 |
| C4 | GND | | | |
| C5 | GND | | | |
| C6 | DP0_M2C_P | M2 | L35P_3 | 42.511 |
| C7 | DP0_M2C_N | M1 | L35N_3 | 41.910 |
| C8 | GND | | | |
| C9 | GND | | | |
| C10 | LA06_P | F9 | L40P_0 | 20.535 |
| C11 | LA06_N | D9 | L40N_0 | 20.818 |
| C12 | GND | | | |
| C13 | GND | | | |
| C14 | LA10_P | B8 | L33P_0 | 12.777 |
| C15 | LA10_N | A8 | L33N_0 | 11.619 |
| C16 | GND | | | |
| C17 | GND | | | |
| C18 | LA14_P | B6 | L4P_0 | 11.501 |
| C19 | LA14_N | A6 | L4N_0 | 10.166 |
| C20 | GND | | | |
| C21 | GND | | | |
| C22 | LA18_P_CC | K3 | L42P_GCLK25_3 | 21.341 |
| C23 | LA18_N_CC | J4 | L42N_GCLK24_3 | 21.307 |
| C24 | GND | | | |
| C25 | GND | | | |
| C26 | LA27_P | B2 | L52P_3 | 11.538 |
| C27 | LA27_N | A2 | L52N_3 | 10.302 |
| C28 | GND | | | |
| C29 | GND | | | |
| C30 | SCL | See FMC system controller section | | |
| C31 | SDA | See FMC system controller section | | |
| C32 | GND | | | |
| C33 | GND | | | |
| C34 | GA0 | See FMC system controller section | | |
| C35 | 12P0V | Connected to TP10 | | |
| C36 | GND | | | |
| C37 | 12P0V | Connected to TP10 | | |
| C38 | GND | | | |
| C39 | 3P3V | Attached to +3.3VDD | | |
| C40 | GND | | | |